REMARKS

This is in full and timely response to the above-identified Office Action. The above listing of the claims supersedes any previous listing. Favorable reexamination and reconsideration are respectfully requested in view of the preceding amendments and the following remarks.

Claim Status

Claims 7-15 remain pending in the application. The claims stand as they were finally rejected.

Rejections under 35 U.S.C. § 102

The rejection of claims 7-10 and 14 under 35 U.S.C. 102(e) as being anticipated by Fang (US 6,667,511) is respectfully traversed.

Rejections under the 35 USC § 102 statute, are based on the premise that to anticipate a claim, each and every element of the claim must be shown in a single reference. When a claimed element cannot be found in the reference, the reference does not anticipate the claimed invention. Further, it is incumbent upon the Examiner to identify where in the reference each element may be found. Ex parte Levy, 17 U.S.P.Q.2d 1461 (Bd. Pat. App. Intrf. 1990). Indeed, when the Examiner fails to identify a claimed element, the Examiner has failed to establish a prima facie case of anticipation.

Fig 9i of Fang discloses, a low voltage transistor 342, a select gate transistor structure 348, a stacked gate flash memory cell structure 346 and a high voltage transistor 350. In this arrangement, the stacked gate flash memory cell structure 346 is formed in a core region, and *the low voltage transistor 342 and the high voltage transistor 350 are formed in a periphery region*.

The claimed invention discloses forming *a code address memory cell including a dielectric layer and a control gate in a periphery circuit region*, and forming a flash memory cell, including a tunnel oxide layer, a floating gate, the dielectric layer and the control gate, in a cell region.

Thus, the periphery circuit region of the claimed invention correspond to the low voltage transistor 342 and the high voltage transistor 350 in the periphery region of Fang.

In the claimed invention, *the dielectric layer is formed between the control gate and the semiconductor substrate*. However, Fang fails to disclose the dielectric layer. Fang shows that *a thin gate oxide 336 is formed between a poly2 gate 338 and a substrate 304 in the low voltage peripheral transistor 342*, and that *a thick gate oxide 337 is formed between the poly2 gate 338 and the substrate 304 in the high voltage peripheral transistor 350*. In Fang, the dielectric layer is formed in the core region, not in the periphery region.

For the reasons discussed *supra*, Applicant respectfully submits that claim 7 is not anticipated by Fang.

Claims 8-10 and 14, which are dependent on claim 7, are patentable for the reasons discussed above with respect to claim 7, as well as on their own merits.

Claim Rejections -35 U.S.C. § 103

The rejection of claims 11-13 and 15 under 35 U.S.C. § 103(a) as being unpatentable over Fang (US 6,667,511) in view of Sheng et al. (US 5,981,404), is respectfully traversed.

Claims 11-12 and 15 are dependent on the base claim 7, which is allowable for the reasons advanced above. Further, Sheng et al. does not supply the above-noted deficiencies of Fang. Thus, claims 11-12 and 15 are patentable for the reasons discussed above with respect to claim 7, as well as on their own merits.

In connection with claim 13, for the same reasons as advanced above in connection with claim 7, Fang fails to disclose that the claimed dielectric layer is formed between the control gate and the semiconductor substrate. Sheng et al. is silent with respect to the dielectric layer being formed between the control gate and the semiconductor substrate. Accordingly, claim 13 is patentable for the reasons discussed above with respect to claim 7, as well as on their own merits. That is to say, in order to establish a *prima facie* case of obviousness, it is necessary to show that the hypothetical person of ordinary skill would, without any knowledge of the claimed subject matter and without any inventive activity, be motivated to arrive at the claimed subject matter given the guidance of the cited references when each is fully considered as statutorily required.

Conclusion

All objections and rejections having been addressed, it is respectfully submitted that

claims 7-15 stand in condition for allowance and a notice to that effect is courteously solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 07-1337 and please credit any excess fees to such deposit account.

Respectfully submitted,
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